Ok I started this really late but here is starting from the esp development

I still need to add everything before this.

ESP – FPGA Communication.

This the test bench for spi communication between the fpga and esp. This is the top level and how it works is the registers r\_spi\_clk, r\_spi\_cs, and r\_spi\_mosi are inputs from the esp32. When CS is high the spi slave code waits for the register r\_spi\_clk to have a rising edge. When a rising edge is for the spi clk happens the the r\_SPI\_MISO is checked if it is 1 then that bit is set to high and if it’s low that bit is set to low. After 8 clocks the spi master code is given the byte and a pulse and it then sends the spi out. This is just purely for testing to see if the FPGA is receiving the spi signals. As you can see below the test bench is working.